UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,715	12/31/2003	Chris J. Newburn	42P18598	1390

8791 7590 09/11/2006

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
FARROKH, HASHEM	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 09/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,715	NEWBURN ET AL.	
	Examiner	Art Unit	
	Hashem Farrokh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-68* is/are pending in the application.

4a) Of the above claim(s) *44-68* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-12,17-27 and 32-43* is/are rejected.

7)☒ Claim(s) *13-16 and 28-31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/7/06,6,7/06*, 8/23/06
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This Office Action is in response to the Applicant's Remarks filed on June 7, 2006; claim 2 has been canceled; claim 1 has been amended; claims 3-68 have been added.

1. Newly submitted claims 44-68 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: Claims 44-68 include snooping a cache, which is distinct from original invention (e.g., compression) and has distinct prior art classification.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 44-68 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

Claims 1, 3, 7, 11, 17-18, 22, 26, 32-34, 38, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,640,283 B2 to Naffziger et al. (hereinafter Naffziger) in view of U.S. Patent 6,735,673 B2 to Kever.

1. In regard to claim 1, Naffziger teaches:

"A memory controller **(e.g., element 106 in Fig. 1; fig. 2)** for use in a system **(e.g., System 100 shown in Fig. 1)** having a program-addressable memory **(e.g., element 110 in Fig. 1)** controlled by the memory controller **(e.g., element 106 in Fig. 1; fig. 2)** and a processor **(e.g., Processor 102 in Fig. 1)** coupled with the memory **(e.g., Main Memory 110 in Fig. 1)** by an external bus," **(e.g., see column 6, line 55-57; element 234 in Fig. 2).** *For example the Level 2 Cache shown as element 106 in Fig. 1 and in more detail in Fig. 2 includes cache and memory controller that is coupled to the external Main Memory by Miss Logic 234 shown in Fig. 2 via an external bus (e.g., indicated in Fig. 2 as To/From Main Memory).*

"the memory controller comprising a compression map cache **(e.g., Tag Memory 304 in Fig. 3)** to store information that identifies a compressed cache line's worth of information stored in the memory," **(e.g., see column 7, line 3-8; Compressed Flags 406 in Fig. 4).** *Naffziger teaches that the cache lines are compressed for releasing free space for reuse (e.g., see column 3, lines 53-54), however Naffziger does not expressly teach:* "the compressed cache line's worth of information comprising a compressed version of a first cache line's worth of information and a compressed version of a second cache line's worth of information."

Kever teaches: "the compressed cache line's worth of information comprising a compressed version of a first cache line's worth of information and a compressed version of a second cache line's worth of information." **(e.g., see Abstract; column 8, line 8 in claim 14)** *for storing two compressed lines of data.*

Disclosures by Naffziger and Kever are analogous because both references teach methods of cache compression.

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the Cache Compression Engine taught by Naffziger to include storing the multiple compressed cache lines disclosed by Kever.

The motivation for compressing and storing multiple cache lines in cache as indicated by column 2, lines 14-15 of Kever would have been to increase the probability cache hit, which results in a processing system performance enhancement.

Therefore, it would have been obvious to combine disclosures by Kever with Naffziger to obtain the invention as specified in the claim.

2. *In regard to claim 17, Naffziger teaches:*

"A processor **(e.g., Processor 102 in Fig. 1)** and a memory controller **(e.g., Level 2 cache 102 in Fig. 1; Fig. 2)** integrated on a same semiconductor die," **(e.g., see column 4, lines 66-67 to column 5, lines 1-8; element 103 in Fig. 1).**

"the memory controller controlling a program-addressable memory coupled with the processor by an external bus," **(e.g., see column 6, line 55-57; element 234 in Fig. 2).**

"the memory controller comprising a compression map cache **(e.g., Tag Memory 304 in Fig. 3)** to store information that identifies a compressed cache line's worth of information stored in the memory," **(e.g., see column 7, line 3-8; Compressed Flags 406 in Fig. 4).** *Naffziger teaches that the cache lines are compressed for releasing free space for reuse (e.g., see column 3, lines 53-54), however Naffziger does not expressly teach:* "the compressed cache line's worth of information comprising a compressed

version of a first cache line's worth of information and a compressed version of a second cache line's worth of information."

Kever teaches: "the compressed cache line's worth of information comprising a compressed version of a first cache line's worth of information and a compressed version of a second cache line's worth of information." **(e.g., see Abstract; column 8, line 8 in claim 14)** *for storing two compressed lines of data. Motivation for combining Naffziger with Kever is based on the same rational given for rejection of claim 1.*

3. In regard to claim 33, Naffziger teaches:

"A computing system **(e.g., Fig. 1)** comprising:"

"a) a program-addressable memory;" **(e.g., Main Memory 110 in Fig. 1).**

"b) a processor and a memory controller integrated on a same semiconductor die," **(e.g., see column 4, lines 66-67 to column 5, lines 1-8; element 103 in Fig. 1).**

"the memory controller controlling the memory **(e.g., column 6, lines 55-62)**, the memory controller comprising a compression map cache **(e.g., Tag Memory 304 in Fig. 3)** to store information that identifies a compressed cache line's worth of information stored in the memory **(e.g., see column 7, line 3-8; Compressed Flags 406 in Fig. 4)**," *Naffziger teaches that the cache lines are compressed for releasing free space for reuse (e.g., see column 3, lines 53-54), however Naffziger does not expressly teach:* "the compressed cache line's worth of information comprising a compressed version of a first cache line's worth of information and a compressed version of a second cache line's worth of information."

Kever teaches: "the compressed cache line's worth of information comprising a compressed version of a first cache line's worth of information and a compressed version of a second cache line's worth of information." **(e.g., see Abstract; column 8, line 8 in claim 14)** *for storing two compressed lines of data. Motivation for combining Naffziger with Kever is based on the same rational given for rejection of claim 1.*

4. In regard to claims 3, 18, and 34 Naffziger further teaches:

"wherein the information comprises a bit for each block of a plurality of blocks of memory space of the memory **(e.g., Compression Flag 406 represents the bit for each cache line)**, wherein each of the plurality blocks stores its own cache line's worth of information **(e.g., see column 7, lines 22-33)**, the bit to indicate whether its corresponding block is storing a compressed cache line's worth of information." **(e.g., see column 7, lines 31-34).** *The cache tag includes a plurality of flags including the compression flag corresponding to each cache line.*

5. In regard to claims 7, 22, and 38 Naffziger further teaches:

"wherein the information comprises a bit for each macro block of a plurality of macro blocks of memory space of the memory **(e.g., Compression Flag 406 represents the bit for each cache line)**, where each macro block of memory space of the memory stores a cache lines' worth of information for a set of companion cache lines' worth of information **(e.g., see column 7, lines 22-33)**, the bit to indicate whether the companion cache lines' worth of information of its corresponding macro block have been compressed." **(e.g., see column 7, lines 31-34).** *The cache tag includes a plurality of flags including the compression flag corresponding to each cache line.*

6. In regard to claims 11, 26, and 42 Naffziger further teaches:

"further comprising a memory space to identify physical continuous addressing space of the memory in which a compression map is stored." **(e.g., see column 7, lines 44-49; Fig 5).** *Naffziger teaches the compression engine has an address pointer that points to the cache tag memory in which the compression map (e.g., compression flags) is stored. The pointer may be implemented using a counter to scan all location within the tag memory. Therefore, the compression map is inherently stored in a continuous space of cache tag memory.*

7. In regard to claim 32 Naffziger further teaches:

"wherein the processor **(e.g., element 106 in Fig. 1)** comprises a cache controller **(e.g., Fig. 2)** with compression logic circuitry," **(e.g., element Compression Engine 230 in Fig. 2)**. *However, Naffziger does not expressly teach:* "the compression logic circuitry to compress the first cache line's worth of information with the second cache line's worth of information to form the compressed cache line's worth of information."

Kever teaches: "the compression logic circuitry to compress the first cache line's worth of information with the second cache line's worth of information to form the compressed cache line's worth of information." **(e.g., see Abstract; column 8, line 8 in claim 14)** *for storing two compressed cache lines of data as a cache line of data.*

Claims 4, 8, 19, 23, 35 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naffziger in view of Kever as applied to claims 3, 7, 18, 22, 34 and 38 above, and further in view of U.S. Patent No. 6,825,847 B1 to Molnar et al. (hereinafter

Molnar).

8. In regard to claims 4, 19, and 35 Naffziger in view of Kever teach information including flags that indicate whether the cache lines are compressed or uncompressed. However neither Naffziger nor Kever teaches: "wherein the information further comprises an indication of the type of compression..."

Molnar teaches: "wherein the information further comprises an indication of the type of compression ..." **(e.g., see column 16, 52-54)** *for indicating in memory whether the samples are stored compressed or uncompressed and a type of compression format.*

Disclosures by Naffziger, Kever, and Molnar are analogous because all references related to memory data compression.

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the Cache Compression Engine taught by Naffziger to include storing the multiple compressed cache lines disclosed by Kever. Furthermore to include an indication of type of compression format in compressing pixel colors (e.g., data) taught by Molnar.

The motivation for compressing and storing multiple cache lines in cache as indicated by column 2, lines 14-15 of Kever would have been to increase the probability cache hit, which results in a processing system performance enhancement. Furthermore, the motivation for compression of fragment data and indicating the compression type as taught by column 1, lines 50-67 is to improve the prior art limitations associated with fragment-processing rate.

Therefore, it would have been obvious to combine disclosures by Molnar with Kever and Naffziger to obtain the invention as specified in the claim.

9. Claims 8, 23, and 39 are rejected base on the same rational given in rejection of claims 4, 19, and 35 above.

Claims 5-6, 9-10, 20-21, 24-25, 36-37 and 40-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naffziger in view of Kever as applied to claims 3, 7, 18, 22, 34, and 38 above, and further in view of U.S. Patent Publication No.2004/0030847 A1 to Tremaine.

10. In regard to claims 5, 9, 20, 24, 36 and 40 Naffziger in view of Kever teach information including flags that indicate whether the cache lines are compressed or uncompressed. However neither Naffziger nor Kever expressly teaches: "wherein, when all bits of the corresponding block is storing a same value, the value is identified in the information."

Tremaine teaches: "wherein, when all bits of the corresponding block is storing a same value **(e.g., see paragraph 38 in page 5)**, the value is identified in the information." **(e.g., see claim 5 in page 7)** *for compression attributes to include a zero attribute indicating a data block of all zeros.*

Disclosures by Naffziger, Kever, and Tremaine are analogous because all references related to memory data compression.

At the time of invention it would have been obvious to a person of ordinary skill in art to

modify the Cache Compression Engine taught by Naffziger to include storing the multiple compressed cache lines disclosed by Kever. Furthermore to include a zero attribute indicator for memory block of all zeros taught by Tremaine.

The motivation for compressing and storing multiple cache lines in cache as indicated by column 2, lines 14-15 of Kever would have been to increase the probability cache hit, which results in a processing system performance enhancement. Furthermore, the motivation for zero attribute indication as taught by paragraph 48, page 2 of Tremaine is to benefit from an overall memory read latency (higher performance.

Therefore, it would have been obvious to combine disclosures by Tremaine with Kever and Naffziger to obtain the invention as specified in the claim.

11. In regard to claims 6, 10, 21, 25, 37, and 41Tremaine further teaches "wherein the value is a value of 0." **(e.g., see paragraph 38 in page 5; claim 5 in page 7)** *for compression attributes to include a zero attribute indicating a data block of all zeros.*

Claims 12, 27, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naffziger in view of Kever as applied to claims 11, 26, and 42 above, and further in view of U.S. Patent Publication No.2003/0233534 A1 to Bernard et al. (hereinafter Bernard).

12. In regard to claims 12, 27, and 43 Naffziger in view of Kever teach all limitations included in the base claims but does not teach: "wherein the memory space is to be written to by a computing system's BIOS."

Bernard teaches: "wherein the memory space is to be written to by a computing system's BIOS." **(e.g., see paragraph 15 in page)** *for reading configuration information from non-volatile memory and writing to memory locations by a BIOS program. Disclosures by Naffziger, Kever, and Bernard are analogous because all references related to memory data management.*

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the Cache Compression Engine taught by Naffziger to include storing the multiple compressed cache lines disclosed by Kever. Furthermore to include a program for reading and writing the configuration information as taught by Bernard.

The motivation for compressing and storing multiple cache lines in cache as indicated by column 2, lines 14-15 of Kever would have been to increase the probability of cache hit, which results in a processing system performance enhancement. Furthermore, the motivation using BIOS as taught by paragraph 40, page 4 of Bernard is to guarantee near-continuous operation and fast booting computer, thus saving time, weight, space, and cost.

Therefore, it would have been obvious to combine disclosures by Bernard with Kever and Naffziger to obtain the invention as specified in the claim.

ALLOWABLE SUBJECT MATTER

Claims 13-16 and 28-31 are objected to as being dependent upon rejected based claims, but would be allowable if rewritten in correct and independent form including all of the limitations of the base claim and any intervening claims.

1. The primary reason for allowance of claims 13 and 28 in instant application is the combination with the inclusion of the following limitations: **a scheduler to schedule** requests made to the memory controller, the scheduler coupled to the compression map cache to refer to the information to determine whether a request's corresponding cache line's worth of information is stored in the memory in a compressed state.

2. The primary reason for allowance of claims 14-29 in instant application is the combination with the inclusion of the following limitations: **a first read path that flows through decompression logic circuitry and a second read path that bypasses the decompression logic circuitry, the decompression logic circuitry to decompress a compressed cache line's worth of information that has been read from the memory when a request's corresponding cache line's worth of information is stored in the memory in a compressed state.**

3. The primary reason for allowance of claims 15-16 and 30-31 in instant application is the combination with the inclusion of the following limitations: **compression logic circuitry coupled to a queue for queuing the requests, the compression logic circuitry to compress an uncompressed cache line's worth of information with a companion of the uncompressed cache line's worth of information.**

Respond to Remarks

As stated above claims 44-68 directed to invention that is distinct from originally submitted invention and therefore are withdrawn in this Office Action.

Conclusion

The prior art made of record and not relied upon are as follows:

1. U. S. Patent Publication No. 2003/0191903 A1 to Sperber et al. describes Memory system for multiple data types.

2. U. S. Patent Publication No. 2004/0161146 A1 to Van Hook et al. describes Method and apparatus for compression of multi-sampled anti-aliasing color data.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication should be directed to Hashem Farrokh whose telephone number is (571) 272-4193. The examiner can normally be reached Monday-Friday from ***8:00 AM to 5:00 PM.***

If attempt to reach the above noted Examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Donald A Sparks, can be reached on (571) 272-4201. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBS) at 866-217-9197 (toll-free).

HF

2006-08-28

Brian R. Peugh
Primary Examiner